Source and Sink 1.5A/2A Fast Transient Response Line Regulator TD5860(A)

General Description

The TD5860/TD5860A linear regulator is designed to provide a regulated voltage with bi-direction output current for DDRSDRAM termination voltage. The TD5860 integrates two power transistors to source or sink load current up to 1.5A/2A. It also features internal soft-start, current-limit, thermal shutdown and enable control functions into a single chip.

The internal soft-start controls the rising rate of the output voltage to prevent inrush current during start-up. The current-limit circuit detects the output current and limits the current during short-circuit or current overload conditions. The on-chip thermal shutdown provides thermal protection against any combination of overload that would create excessive junction temperatures.

The output voltage of TD5860/TD5860A is regulated to track the voltage on VREF pin. An proper resistor divider connected to VIN, GND, and VREF pins is used to provide a half voltage of VIN to VREF pin. In addition, connect an external ceramic capacitor and a open-drain transistor to VREF pin for external soft-start and shutdown control.

Pulling and holding the voltage on VREF below the enable voltage threshold shuts down the output. The output of TD5860/TD5860A will be high impedance after being shut down by VREF or the thermal shutdown function.

Features

- Provide Bi-direction Output Currents
- Sourcing and Sinking Current up to 1.5A/2A Built-in Soft-Start
- Power-On-Reset Monitoring on VCNTL and VIN pins
- Fast Transient Response
- Stable with Ceramic Output Capacitors ±20mV High System Output Accuracy over Load and Temperature Ranges
- Adjustable Output Voltage by External Resistors
- Current-Limit Protection
- On-Chip Thermal Shutdown
- Shutdown for Standby or Suspend Mode
- SimpleSOP-8 with Exposed Pad(SOP8-PP) Packages
- Lead Free and Green Devices Available(RoHS Compliant)

Applications

- DDRII/III SDRAM Termination Voltage
- Motherboard and VGA Card Power Supplies
- Setop Box
- SSTL-2/3 Termination Voltage

Package Types

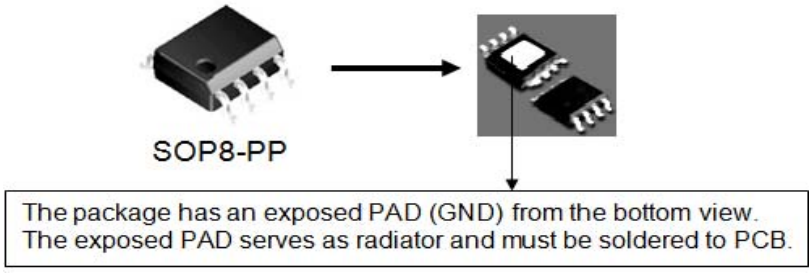


Figure 1 Package Types of TD5860/TD5860A

Pin Configurations

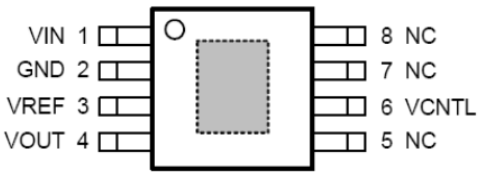
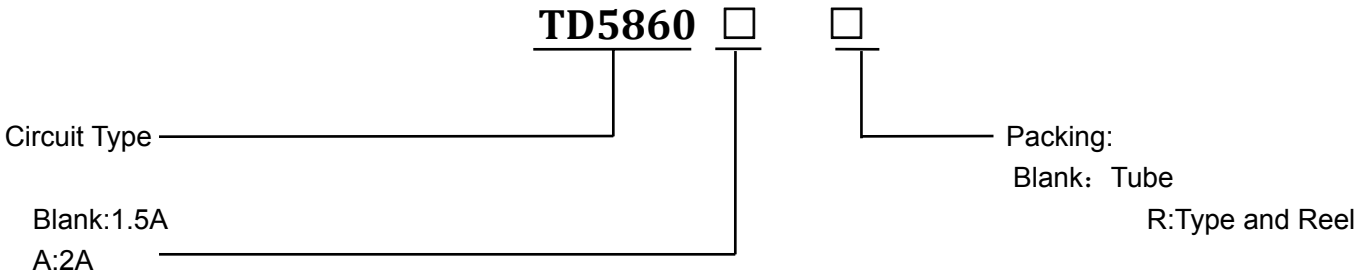


Figure 2 Pin Configuration of TD5860/TD5860A (Top View)

Pin Description

Pin Number	Pin Name	Description
1	VIN	Main Power Input Pin. Connect this pin to a voltage source and an input capacitor. The TD5860/TD5860A sources current to VOUT pin by controlling the upper pass MOSFET, providing a current path from VIN to VOUT.
2	GND	Power and Signal Ground. Connect this pin to system ground plane with shortest traces. The TD5860/TD5860A sinks current from VOUT pin by controlling the lower pass MOSFET, providing a current path from VOUT to GND. This pin is also the ground path for internal control circuitry.
3	VREF	Reference Voltage Input and Active-high Enable Control Pin. Apply a voltage to this pin as a reference voltage for the TD5860/TD5860A. Connect this pin to a resistor diver, between VIN and GND, and a capacitor for filtering noise purpose. Applying and holding the voltage below the enable voltage threshold on this pin by an open-drain transistor shuts down the output. During shutdown, the VOUT pin has high input impedance.
4	VOUT	I Output Pin of The Regulator. Connect this pin to load and output capacitors (>8μF MLCC is necessary) required for stability and improving transient response. The output voltage is regulated to track the reference voltage and capable of sourcing or sinking current up to 1.5A/2A.
5,7,8	NC	No Internal Connection.
6	VCNTL	Power Input Pin for Internal Control Circuitry. Connect this pin to a voltage source, providing a bias for the internal control circuitry. A decoupling capacitor is connected near this pin.
Exposed Pin	GND	Chip Substrate Connection of The Chip. Connect this pad to system ground plane for good thermal conductivity.

Ordering Information



Absolute Maximum Ratings

Note1: Stresses greater than those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Parameter	Symbol	Value	Unit
VCNTL Supply Voltage(VCNTL to GND)	V_{CNTL}	-0.3 to 7	V
VIN Supply voltage(VIN to GND)	V_{IN}	-0.3 to 7	V
VREF Input Voltage(VREF to GND)	V_{REF}	-0.3 to 7	V
VOUT Output Voltage(VOUT to GND)	V_{OUT}	-0.3 to Vin+0.3	V
Power Dissipation	P_D	Internally Limited	mW
Operating Junction Temperature	T_J	150	ºC
Storage Temperature	T_{STG}	-65 to 150	ºC
Lead Temperature (Soldering, 10 sec)	T_{LEAD}	260	ºC
ESD (HBM)		2000	V
MSL		Level3	
Thermal Resistance-Junction to Ambient	RθJA	55	ºC / W
Thermal Resistance-Junction to Case	RθJC	20	ºC / W

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
VCNTL Supply Voltage	V_{CNTL}	3	5.5	V
VIN Supply Voltage	V_{IN}	1.2	5.5	V
VREF Input Voltage	V_{REF}	0.7	V_{CNTL}-2.2	V
VOUT Output Voltage	V_{OUT}		$V_{REF}\pm0.02$	V
VOUT Output Current(TD5860)	I_{OUT}	-1.5	1.5	A
VOUT Output Current(TD5860A)		-2	2	
Capacitance of Input Capacitor	C_{IN}	10	100	uF
Equivalent Series Resistor(ESR) of Input Capacitor		0	200	mΩ
Capacitance of Output Multi-layer Ceramic Capacitor(MLCC)	C_{OUT}	8	47	uF
Total Output Capacitance		10	330	uF
Operating Junction Temperature	T_J	-40	125	ºC
Operating Ambient Temperature	T_A	-40	85	ºC

Electrical Characteristics

Refer to the typical application circuit. These specifications apply over V_{CNTL}=5V, V_{IN}=1.8V or 1.5V, V_{REF}=0.5V_{IN}, C_{IN}=10μF, C_{OUT}=10μF (MLCC) and T_A= -40~85°C, unless otherwise specified. Typical values are at T_A=25°C.

Parameters	Symbol	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY CURRENT						
VCNTL Supply Current	I_{CNTL}	IOUT=0A		1	2	uA
		VREF=0V(Shutdown)			5	uA
VIN Supply Current at Shutdown	I_{FB}	V_{REF}=GND(Shutdown)			5	uA
POWER-ON-RESET(POR)						
Rising VCNTL POR Threshold		VCNTL Rising	2.5	2.75	2.9	V
VCNTL POR Hysteresis				0.35		V
Rising VIN POR Threshold		VIN Rising	0.7	0.9	1.05	V
VIN POR Hysteresis				0.3		V
OUTPUT VOLTAGE						
VOUT Output Voltage	V_{OUT}	I_{OUT}=0A,V_{REF}=0.7~2.8V		V_{REF}		V
System Accuracy		Over temperature and load current ranges	-20		20	mV
VOUT Offset Voltage(V_{OUT}-V_{REF})	V_{OS}	I_{OUT}=10mA	-7	-1		mV
		I_{OUT}=-10mA		8	12	
Load Regulation		I_{OUT}=10mA~1.5A	-13	-8		mV
		I_{OUT}=-10mA~-1.5A		4	8	

Electrical Characteristics(Cont.)

Refer to the typical application circuit. These specifications apply over V_{CNTL}=5V, V_{IN}=1.8V or 1.5V, V_{REF}=0.5V_{IN}, C_{IN}=10μF, C_{OUT}=10μF (MLCC) and T_A= -40~85°C, unless otherwise specified. Typical values are at T_A=25°C.

Parameters	Symbol	Test Condition		Min.	Typ.	Max.	Unit
PROTECTIONS							
Current-Limit(TD5860 TD5860A)	I_{LIM}	Sourcing Current(V_{IN} =1.8V)	T_J=25℃	1.8 2.2	2 3	3 4	A
			T_J=125℃	1.6 2			
		Sinking Current(V_{IN} =1.8V)	T_J=25℃	-2 -3	-2.2 -2.8	-3 4	
			T_J=125℃	-1.6 -2			
		Sourcing Current(V_{IN} =1.5V)	T_J=25℃	1.6 -2	1.8 -2.2	2.0 3	A
			T_J=125℃	1.1 1.4			
		Sinking Current(V_{IN} =1.5V)	T_J=25℃	-1.6 -2	-1.8 -2.2	-2.6 -3.6	
			T_J=125℃	-1.1			
Thermal Shutdown Temperature	T_{SD}	T_J rising			150		℃
Thermal Shutdown Hysteresis					40		
VREF Enable Voltage Threshold				0.15	0.3	0.4	V
VREF Bias Current	I_{VREF}			-100		100	nA
Soft-Start Interval	T_{SS}			0.1	0.2	0.4	ms

Type Application Circuit

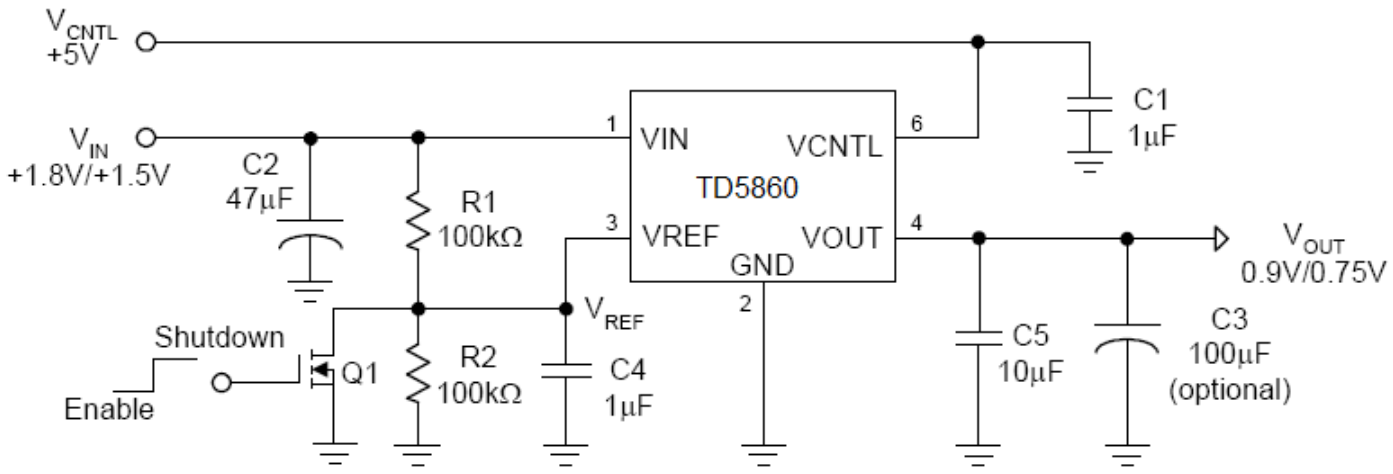
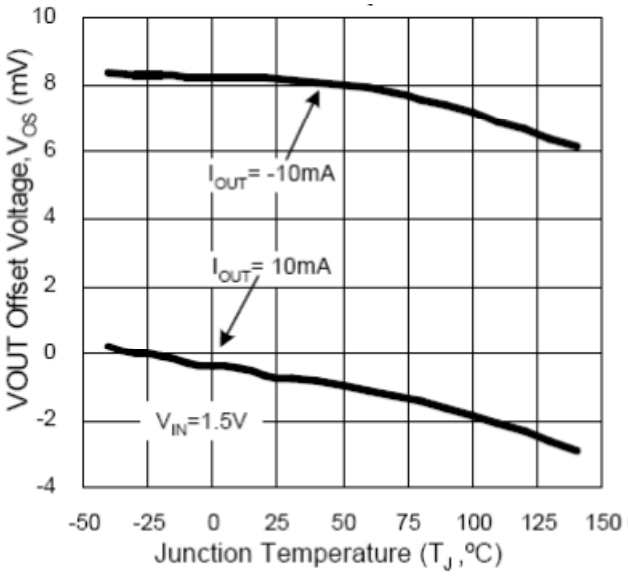


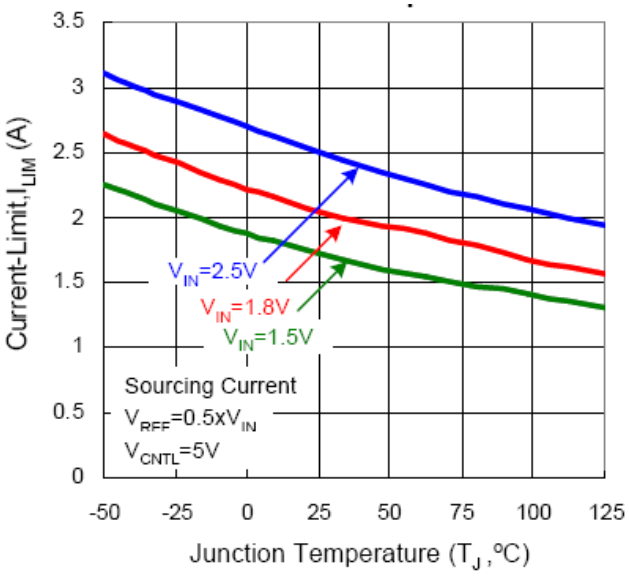
Figure 3. Type Application Circuit of TD5860/TD5860A

Typical Operating Characteristics

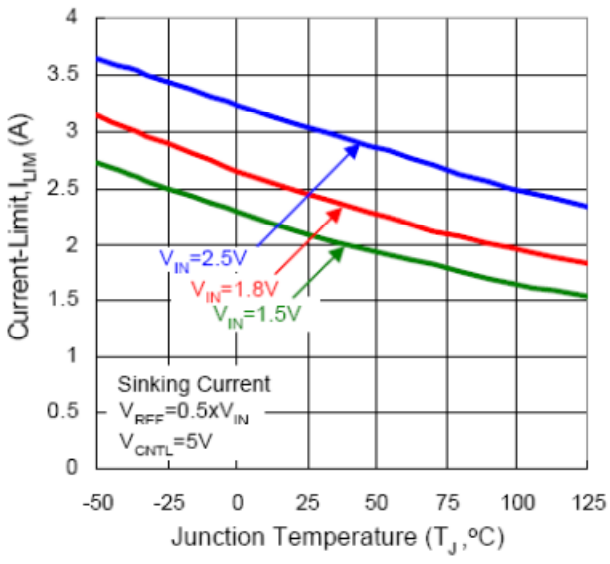
VOUT Offset Voltage vs. Junction Temperature



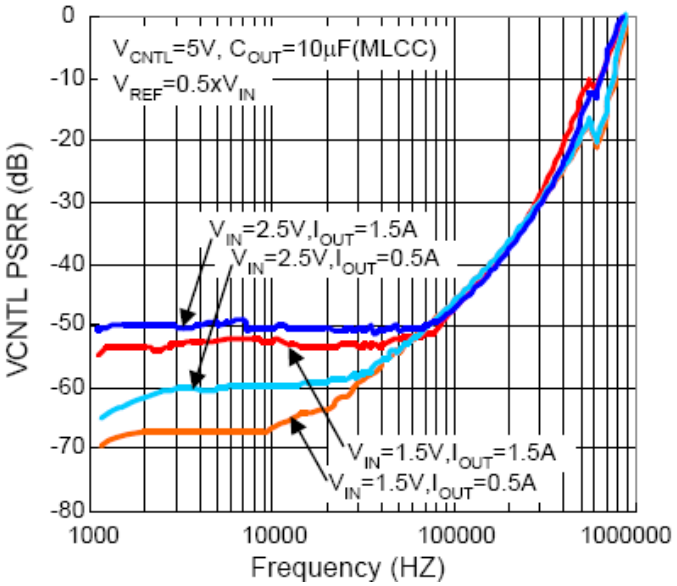
Sourcing Current-Limit vs. Junction Temperature



Sinking Current-Limit vs. Junction Temperature

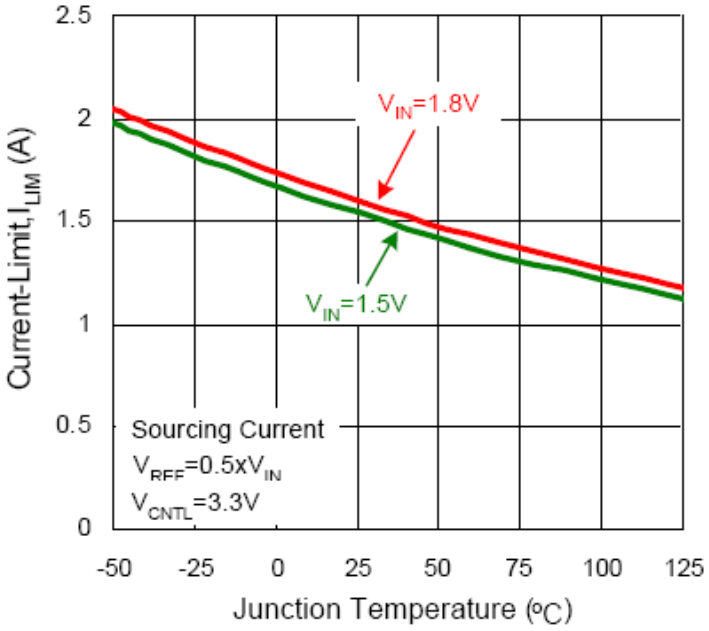


VCNTL Power Supply Rejection Ratio (PSRR)

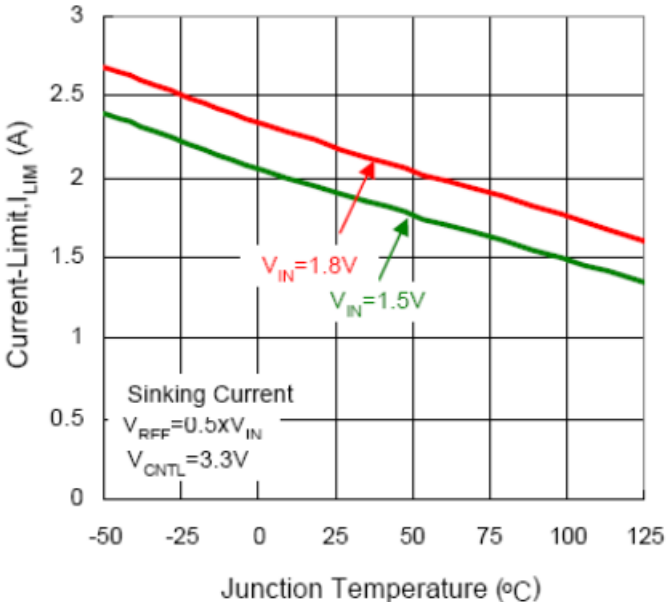


Typical Operating Characteristics(Cont.)

Sourcing Current-Limit vs. Junction Temperature



Sinking Current-Limit vs. Junction Temp



Function Description

Power-On-Reset

A Power-On-Reset (POR) circuit monitors both input voltages at VCNTL and VIN pins to prevent wrong logic ontrols. The POR function initiates a soft-start process fter both of the supply voltages exceed their rising POR oltage thresholds during powering on.

Output Voltage Regulation

The output voltage on VOUT pin is regulated to track the eference voltage applied on VREF pin. Two internal Nchannel ower MOSFETs controlled by high bandwidth ror amplifiers regulate the output voltage by sourcing urrent from VIN pin or sinking current to GND pin. An nternal output voltage sense pad is bonded to the VOUT in with a bonding wire for perfect load regulation.For preventing the two power MOSFETs from shootthrough, small voltage offset between the positive inputs f the two error amplifiers is designed. It results in igher output voltage while the regulator sinks light or eavy load current.

The TD5860/TD5860A provides very fast load transient response t small output capacitance to save total cost.

Current-Limit

The TD5860/TD5860A monitors the output current, both sourcing nd sinking current, and limits the maximum output current o prevent damages during current overload or shortcircuit shorted from VOUT to GND or VIN) conditions.

Enable

during continuous thermal overload conditions, increasing lifetime of the TD5860/TD5860A.

The VREF pin is a multi-function input pin which is the reference voltage input pin and the enable control input pin. Applying and holding the voltage (VREF) on VREF below 0.3V (typical) shuts down the output of the regulator. In the typical application, an NPN transistor or N-channel MOSFET is used to pull down the VREF while applying a “high” signal to turn on the transistor. When shutdown function is active, both of the internal power MOSFETs are turned off and the impedance of the VOUT pin is larger than 10MΩ.

Internal and External Soft-Start

The TD5860/TD5860A is designed with an internal soft-start function to control the rise rate of the output voltage to prevent inrush current during start-up.

When release the pull-low transistor connected with VREF pin, the current via the resistor divider charges the external soft-start capacitor (C4) and the VREF starts to rise up.The IC starts a soft-start process when the VREF reaches the enable voltage threshold. The output voltage is regulated to follow the lower voltage, which is either the internal soft-start voltage ramp or the VREF voltage, to rise up. The external soft-start interval is programmable by the resistor-divider and the soft-start capacitor (C4).

Thermal Shutdown

The thermal shutdown circuit limits the junction temperature of the TD5860/TD5860A. When the junction temperature exceeds 150oC, a thermal sensor turns off the both pass transistors, allowing the device to cool down. The thermal sensor allows the regulator to regulate again after the junction temperature cools by 40oC, resulting in a pulsed output during continuous thermal overload conditions. The thermal limit is designed with a 40oC hysteresis to lower the average TJ

Application Information

Power Sequencing

The input sequence of powers applied for VIN and VCNTL is not necessary to be concerned.

Reference Voltage

A reference voltage is applied at the VREF pin by a resistor divider between VIN and GND pins. An external bypass capacitor is also connected to VREF. The capacitor and the resistor divider form a low-pass filter to reduce the inherent reference noise from VIN. The capacitor is a 0.1μF or greater ceramic capacitor and connected as close to VREF as possible. More capacitance and large resistor divider will increase the soft-start interval. Do not place any additional loading on this reference input pin

Input Capacitor

The TD5860/TD5860A requires proper input capacitors to supply current surge during stepping load transients to prevent the input rail from dropping. Because the parasitic inductors from the voltage sources or other bulk capacitors to the VIN pin limit the slew rate of the input current, more parasitic inductance needs more input capacitance. For the TD5860, the total capacitance of input capacitors value including MLCC and aluminum electrolytic capacitors should be larger than 10μF. For VCNTL pin, a capacitor of 0.47μF (MLCC) or above is recommended for noise decoupling.

Output Capacitor

The TD5860/TD5860A needs a proper output capacitor to maintain circuit stability and improve transient response. In order to insure the circuit stability, a 10μF X5R or X7R MLCC output capacitor is sufficient at all operating temperatures and it ***must be*** placed near the VOUT. The maximum distance from output capacitor to VOUT must within 10mm. Total output capacitors value including MLCC and aluminum electrolytic capacitors should be larger than 10μF

Table 1 provides the suitable output capacitors for TD5860

Vendor	Description
Murata	10μF, 6.3V, X7R, 0805, GRM21BR70J106K
	10μF, 6.3V, X5R, 0805, GRM21BR60J106K

Operation Region and Power Dissipation

The TD5860/TD5860A maximum power dissipation depends on the thermal resistance and temperature difference between the die junction and ambient air. The power dissipation PD across the device is:

$$P_D \le \frac{(T_J - T_A)}{\theta_{JA}}$$

Where (TJ-TA) is the temperature difference between the junction and ambient air. θJA is the thermal resistance between junction and ambient air. Assuming the TA=25oC and maximum TJ=150oC (typical thermal limit threshold), the maximum power dissipation is calculated as:

$$P_{D(max)} = \frac{(150-25)}{80}$$
$$= 1.56(W)$$

For normal operation, do not exceed the maximum junction temperature of TJ = 125oC. The calculated power dissipation should less than:

$$P_D = \frac{(125-25)}{80}$$
$$= 1.25(W)$$

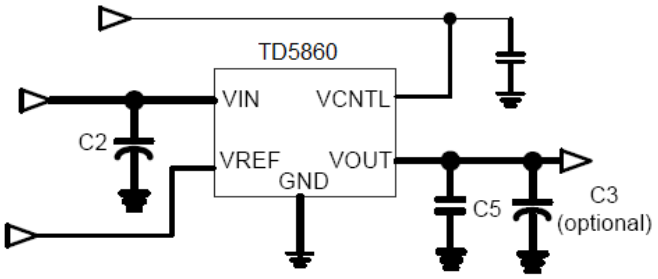


Figure 4

PCB Layout Consideration

Figure 1 illustrates the layout. Below is a checklist for your layout:

1. Please place the input capacitors close to the VIN.
2. Please place the output capacitors close to the VOUT,

a MLCC capacitor larger than 8μF ***must be*** placed near the VOUT. The distance from VOUT to output MLCC must be less than 10mm.

3. To place TD5860/TD5860A and output capacitors near the load is good for load transient response.
4. Large current paths, the bold lines in Figure 4, must have wide tracks.
5. For SOP-8P package, please solder the thermal pad to the TD5860/TD5860A to top-layer ground plane. Numerous

vias 0.254mm in diameter should be used to connect both top-layer and internal ground planes. The ground planes and PCB form a heat sink to channel major power dissipation of the TD5860/TD5860A into ambient air.

Large ground plane is good for heatsinking. Optimum performance can only be achieved when the device is mounted on a PC board according to the board layout diagrams which are shown as Figure 5.

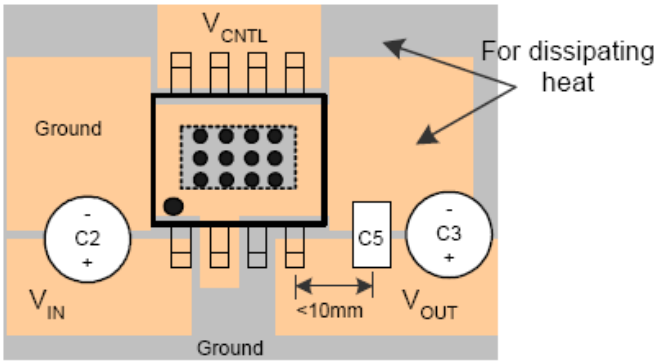
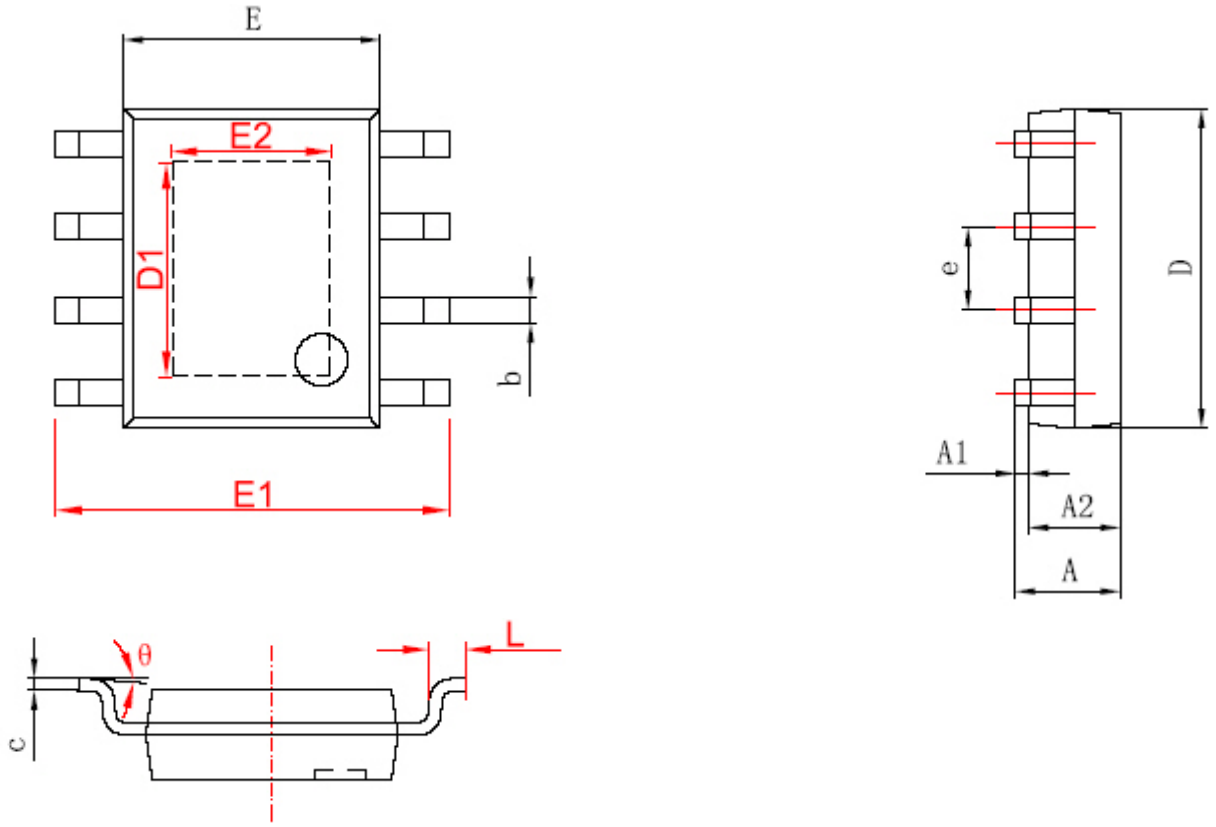


Figure5

Package Information

SOP8-PP Package Outline Dimensions



	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.150	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Design Notes